A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses

Application Note 1591

This application note covers new tools and measurement techniques for characterizing and validating signal integrity of DDR (double data rate synchronous dynamic random access memory) signals.

For simplicity, all DDR1, DDR2, DDR3 and other DDR technologies (including the SDRAM side of fully buffered DIMM) are referred to as DDR in this application note, since each of them has similar electrical characteristics.

Who should read this application note?
Memory designers and test engineers working on high-speed DDR memory buses will find the application note helpful.

Introduction
The trend in DDR memory technology today is towards higher data rates and lower voltage levels. As speeds increase, the validation effort increases dramatically. For a memory system to function accurately, its signal integrity performance must meet certain minimum requirements. Signal integrity is the key to system interoperability, or the guarantee that devices from different vendors will function when they are used together. Failures in signal integrity are closely correlated to other failures, including marginal timing relationships, protocol violations, clock integrity issues and errors from other buses.

The fact that data transfer is bi-directional on the same data bus makes DDR validation a challenge. To analyze the signal integrity performance of DDR signals, it is essential to separate the complex traffic on the data bus. This separation is required to independently analyze the signal characteristics, which are driven from the root complex and DDR chip.

The traffic consists of read data (output), write data (input) and high-impedance (idle) states. Eight data buses constitute one data group, which is source-synchronous to one strobe signal. The write data is shifted 90 degrees from the read data with reference to the strobe signal edges.

You want to be able to easily separate the read-write bits so you can quickly test, debug and resolve signal issues. After the successful separation, engineers frequently use an eye-diagram analysis to check whether the DDR signals meet the voltage, timing and jitter requirements.

In this application note, we will first discuss a few conventional methods for separating complex traffic for analysis. Later, we will outline a few new techniques using the Agilent N5414A InfiniiScan software identification tool that can save you time and give you greater insight into your signals.

Figure 1. The DDR traffic consists of read bursts, write bursts and idle states. For read bursts, the edges of DQS and DQ are aligned, while for the write burst, the DQS is centered of the DQ.

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Conventional method 1: Read-write preamble-width trigger

You can isolate data signals by triggering on the read or write preamble width. From the specification, the read preamble width ranges from 0.9 to 1.1 of one clock cycle period. On the other hand, write preamble width is specified to be larger than 0.35 of one clock cycle period and it has no upper limit. Thus, you need to first determine the preamble width before setting the trigger conditions. Because the preamble has a distinctive width, this method can separate the read and write data.

However, there are challenges with this method. First, the preamble width is loosely defined; it varies with different ASIC/DIMM vendors. Since the upper limit for the write preamble is not defined, it could have the same width as the read preamble. If their values are too close, separating the read and write signals is difficult.

Secondly, a write signal with a preamble of 0.5 clock cycles has a width similar to one data bit period.

The hardware trigger cannot differentiate the write preamble bit from the normal bit.

Thirdly, as DDR data rates get faster, clock periods get narrower. As the clock periods get narrower, the preamble width for the write signal will be greatly reduced. Take DDR3-1600 for example: the minimum preamble width is about 200 ps. A scope hardware trigger might not be able to trigger on such a narrow pulse width.

Figure 2. Trigger on the preamble bit of the DQS-read signal

Figure 3. Trigger on the preamble bit of the DQS-write signal

Conventional method 2: Trigger on amplitude

Usually, the read and write signals have different amplitudes. You can isolate them by triggering on the larger amplitude. However, the larger amplitude is not exclusive to the read or write signal.

Although you can analyze the larger signal, you have no control of the signal you want to analyze. It could also be a problem when both the read and write signals have similar amplitude levels.

Figure 4. Separating the read and write signals based on the signal amplitude. In this case, you can only separate the read signal because the read signal amplitude is slightly higher than the write signal.

Conventional method 3: Isolate read/write cycles using mixed signal oscilloscopes (MSO)

DDR consists of many control signal lines. By connecting the control signals to the MSO's digital inputs, you can trigger on different operation modes (read, write, etc). Different control lines are flagged during each operation. The scope is set to trigger on read or write operation so you can observe the data signals that are connected to the analog input channels.

However, the MSO solution has low bandwidth, usually 1 GHz and below. It is suitable for DDR1 signal measurements, but it does not have the bandwidth for the higher data rates in DDR2 or DDR3 memory devices. Insufficient bandwidth will cause the signal to be distorted, which means your analysis will be inaccurate. So, the challenge is using the limited four channels of a higher-bandwidth scope to separate the read and write signals for higher data rates. Otherwise, an MSO is a perfect solution for DDR signal debugging.

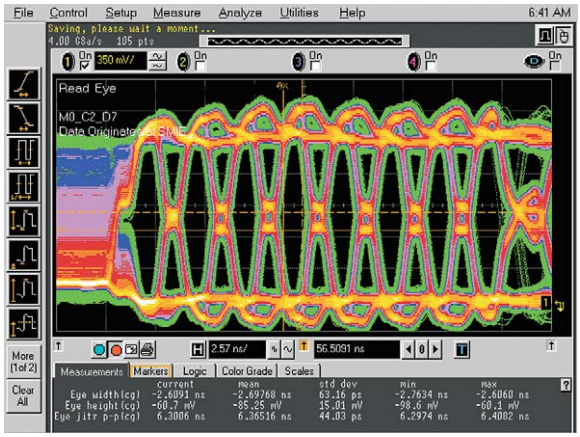

Figure 5. Use the MSO to trigger on control signals to separate the read and write signals.

New method: InfiniiScan zone qualify

Many engineers are frustrated with current methods because they spend too much time trying to set up their scopes to isolate the read-write signals to analyze them independently. Even after they have managed to set up their scopes, consistency and repeatability of the measurements are still low.

Agilent's InfiniiScan software identification tool simplifies DDR validation

With the InfiniiScan zone qualify trigger mode, you can use up to four zones of different sizes to track signals on the scope display. You can set each of these zones to either "Must Intersect" or "Must Not Intersect."

Using the zones, you can track the signal of interest depending on whether the waveform intersects or does not intersect the zones.

In Figure 6, the DDR signal shows a distinctive read and write signal pattern in infinite persistence mode. The DQS signal is the yellow waveform and the DQ signal is green. When the trigger is set on the DQS signal, the DQ shows that the read and write signal pattern overlap each other. So, if you know where to draw the zones, you can easily separate the read and write patterns with InfiniiScan. Using this method, there are no rules on how to use the zones to separate the read or write signals. It all depends on your creativity.

Figure 6. The DDR signal shows a distinctive read and write signal pattern in infinite persistence mode.

New method: InfiniiScan zone qualify *(continued)*

How to separate read signals

First, draw a “Must Not Intersect” zone on the DQS waveform before the trigger point so your scope does not track any normal bits or a high-impedance state.

Once accomplished, you will be able to track the preamble bit consistently, which is the start of the read and write bursts. The read and write signals are still overlapping each other, but you can observe two distinctive DQS waveforms. One of them belongs to the read signal burst.

Draw another zone with “Must Intersect” setting for the lower waveform at the preamble bit. Now, you will be able to distinguish the read burst. Next, you can check whether the DQS-read and DQ-read meet the signal requirements.

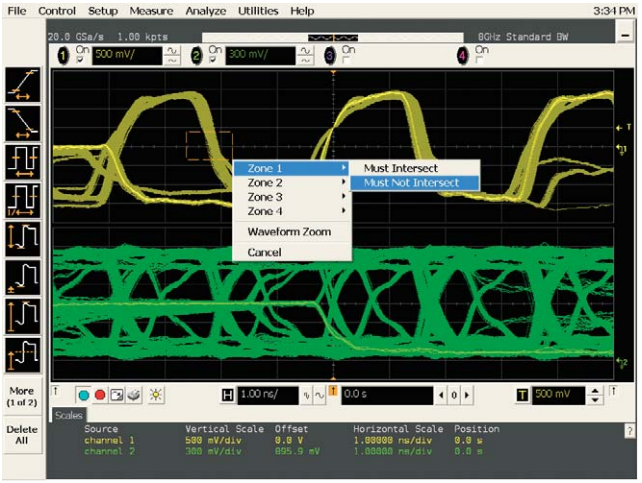

Figure 7. A “Must Not Intersect” zone is drawn on the DQS waveform to discard the data or idle state signals.

Figure 8. With the “Must Not Intersect” zone drawn, the scope consistently tracks the preamble bits of the read and write signals.

Figure 9. Draw a “Must Intersect” zone at the lower waveform at the preamble bit to track the read only signals.

New method: InfiniiScan zone qualify *(continued)*

How to separate write signals

You are now able to track the beginning of the read and write burst by using a "Must Not Intersect" zone. To track the write signal, simply draw a "Must Intersect" zone at the other distinctive waveform – the upper waveform at the preamble bit.

Similarly, you can check whether the DQS-write and DQ-write meet the signal requirements once you successfully separate the read-write signals.

Conclusion

Using the new InfiniiScan software identification method, DDR memory designers and engineers no longer have to face the hassles and difficulties of triggering on read or write data. Engineers who use this time-saving method reap the rewards of faster debug and greater insight into system performance.

Figure 10. The write signal is successfully separated from the complex read-write waveforms.

Related literature

Publication title	Publication type	Publication number
Improve Your Time-to-Insight: Debugging Intermittent Memory Failures in DDR and DDR2 Systems	Application Note	5989-4991EN
N5413A DDR2 Compliance Test Application for Infiniium 54850 and 80000 Series	Data Sheet	5989-3195EN
InfiniiScan Event Identification Software for Infiniium Series Oscilloscopes (N5414A and N5415A)	Data Sheet	5989-4605EN
Infiniium DSO80000B Series Oscilloscopes and InfiniiMax Series Probes	Data Sheet	5989-4606EN
Infiniium 90000 Series Oscilloscopes	Data Sheet	5989-7819EN

Product Web site

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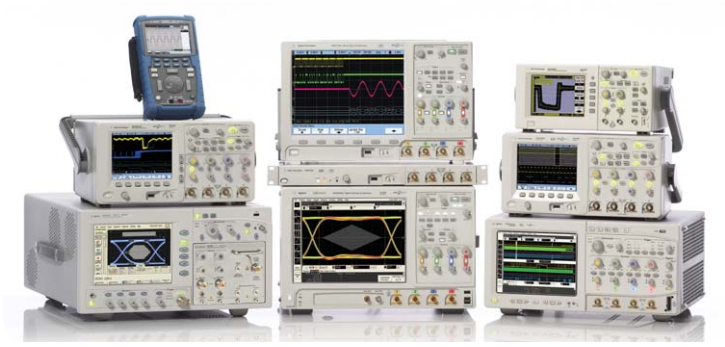

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